CONTROL DATA
CORPORATION

CONTROL DATA®
CYBER 170 MODELS 172/173/174/175
COMPUTER SYSTEMS

INPUT/OUTPUT SPECIFICATIONS

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or use Comment Sheet in the back of this manual.

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INTRODUCTION 1

This specification gives detailed information for the data channels used on the CONTROL DATA® CYBER 170 (Models 172/173/174/175) Computer Systems.

CHANNEL CHARACTERISTICS 2

The CYBER 170 series computer systems are configured with either 10 or 20 separate peripheral processors (PPs),any one of which can exchange data with external equipment connected to a data channel. A 10-PP system allows any processor access to any one of 12 data channels. A 20-PP system allows any of its processors access to any one of 24 data channels. Communication between a processor and an external equipment is via a synchronizer. Signal transfer between a data channel and a controller is by means of one-shot pulses that are converted, within the synchronizer, to the form required by the external equipment.

Each data channel has a 13-bit bidirectional register and several bidirectional control designators that define the status of the register and channel. Each data channel transfers 12-bit words and a parity bit at rates up to a maximum of one word every 500 nanoseconds when the PP is running at 2X speed. The one exception in which a 2MHz transfer rate cannot be maintained occurs in a 20-PP system when a PP on one chassis is accessing a channel on the other chassis and, at the same time, a PP in the second chassis is executing channel instructions; e.g., PP-1 accessing channel 24_8 while PP-13_8 is also performing channel operations. In these exceptional cases, both PPs will operate at the 1MHz rate.

Pulse communication is used on all data and control lines of a channel, all lines are synchronized to the PP clock system, and all channels may be in operation at the same time.

A 'channel active' designator is set from an internal (PP) source, or from an external synchronizer, to reserve a channel for communication between a PP and a synchronizer (or another PP).

A 'channel inactive' designator, originating either internally or externally, clears the 'channel active' designator to terminate communication.

A 'channel full' designator, set from an internal or external source, indicates that a 12-bit (plus parity) data word has been entered into the channel register.

A 'channel empty' signal clears the 'channel full' designator, which in turn clears the channel register.

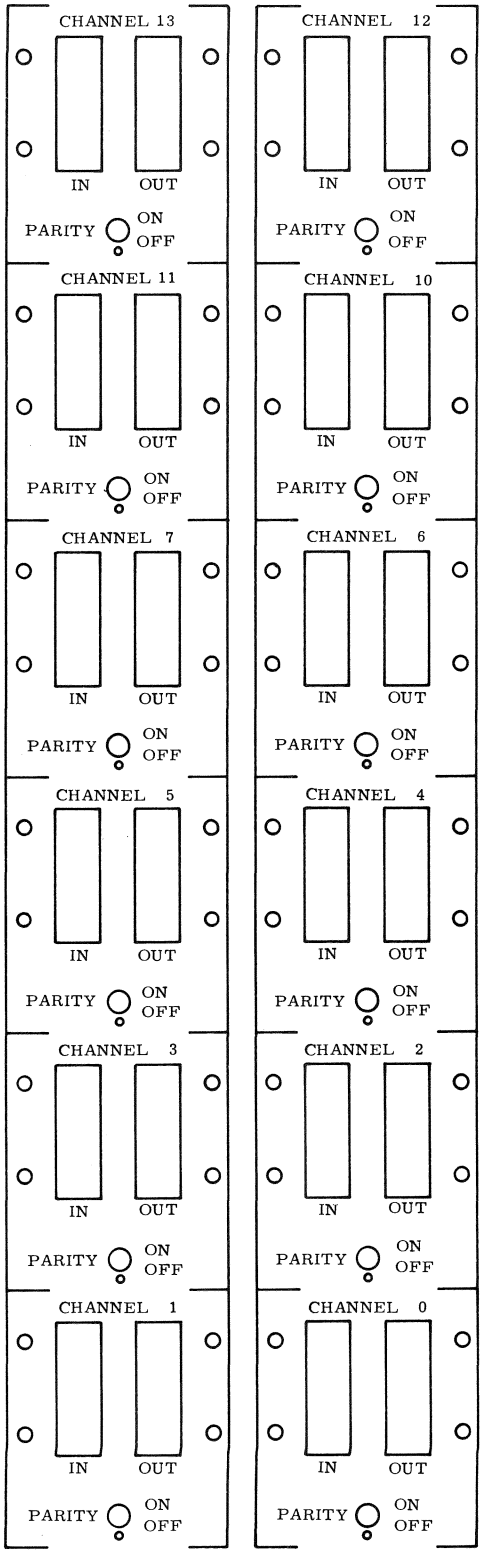


Figure 2-1. Data Channel Cable Connectors

The pulses on the data and control lines are one-shot, nonrepeat type transmissions, and all synchronizers must provide storage for the information. Control signals include a 10MHz (100-nsec period) clock, a 1MHz (1-μsec period) clock, and a MASTER CLEAR for all external devices.

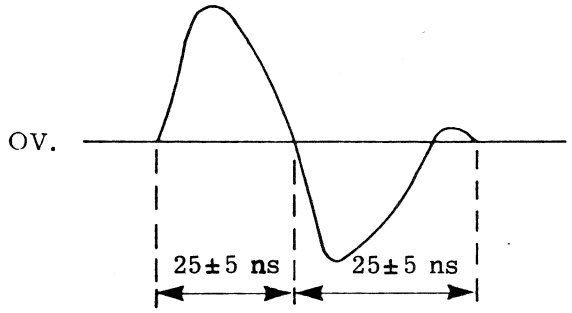
Channel data and control lines are grouped into two cables: input and output (refer to Figure 2-1). The output cables carry processor signals to the synchronizers. The input cables carry synchronizer signals to the processor and the two clocks in the opposite direction. All devices on a channel connect to the data and control lines in a serial-parallel arrangement. Each synchronizer (with the exception of the Data Channel Converter) samples the lines and unconditionally relays all signals to the next-in-line synchronizer. Each synchronizer times the signal relay on the 10MHz clock signal so that all are synchronous with the processor, but time-displaced from each other by one or more clock periods. The Data Channel Converter (DCC) relays data only when not selected (the DCC does relay the function which selects it).

On a CYBER 170 with 10 PPs, channel 10_8 is permanently wired to the Display Controller so that I/O channel data is available to external equipment only via the 'pass-on' logic in the Display Controller. Thus, all I/O transfers on channel 10_8 are delayed by 100 nanoseconds. Channel 10_8 is wired as a normal channel on the second chassis of a 20-PP system when a second Display Controller is not installed.

DATA CHANNEL SIGNAL SPECIFICATIONS

The data channel signal specifications are listed in Table 2-1. Separate input and output cables are used for each data channel. Each cable line originates and terminates on the PPS logic chassis. Cable lines have a fixed length of 75 feet (including the lengths internal to both the PPS and external synchronizer.

A logical '1' signal, measured at the circuit terminals of the sending device, is illustrated in Figure 2-2 and described in Table 2-2. No signal is impressed on the line for a logical '0'. Input circuits in the external equipment must terminate the line in its characteristic impedance.



MAX VOLTAGE SWING = ± 2.7V p-p
MIN VOLTAGE SWING = ± 2.1V p-p

Figure 2.2 Output Pulse Characteristics

Measured at output pin of TR. looking into a 75Ω impedance.

TABLE 2-1. DATA CHANNEL COAXIAL CABLE LINES

Input Cable	PIN	Color Code	Output Cable
Data 2^0	A	90	Data 2^0
Data 2^1	B	91	Data 2^1
Data 2^2	C	92	Data 2^2
Data 2^3	D	93	Data 2^3
Data 2^4	E	94	Data 2^4
Data 2^5	F	95	Data 2^5
Data 2^6	H	96	Data 2^6
Data 2^7	J	97	Data 2^7
Data 2^8	K	98	Data 2^8
Data 2^9	L	99	Data 2^9
Data 2^{10}	M	900	Data 2^{10}
Data 2^{11}	N	901	Data 2^{11}
Active	P	902	Active
Inactive	R	903	Inactive
Full	S	904	Full
Empty	T	905	Empty
Clock (10 mc)	U	906	Function
Clock (1 mc)	V	907	Master Clear
Input Data Parity	W	908	Output Data Parity

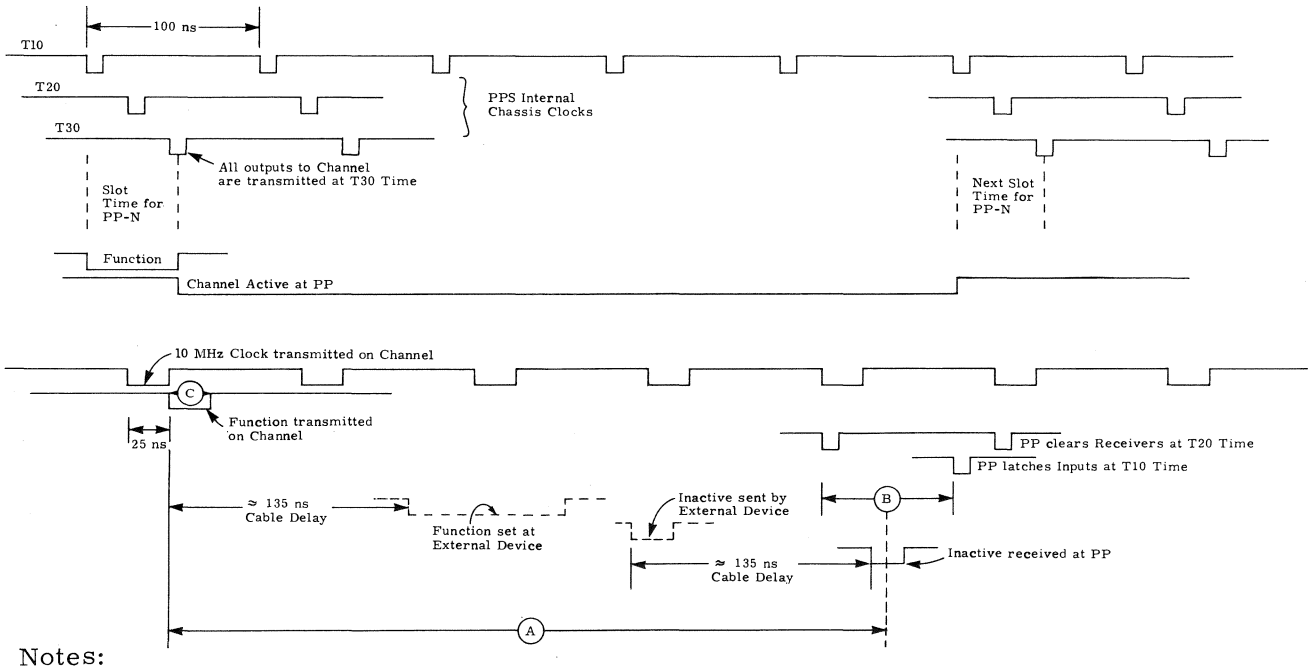
TABLE 2-2. LINE CHARACTERISTICS

Parameter	Description
Line length (maximum)	75 feet (typical CDC cable)
Pulse amplitude at output of the transmitter	2.3 volt peak at 32 milliamperes into a 70-73 ohm coaxial cable - the cable to be terminated in its approximate characteristic impedance
Rise time (at the output of the transmitter)	2 nanoseconds
Fall time (at the output of the transmitter)	2 nanoseconds
Line capacitance	21.5 picofarad/foot maximum (typical CDC cable)
Line attenuation	0.045 decibel/foot (typical)
Voltage rating	30 volts maximum

NOTE

75 feet line length is the total length from the transmitter to the receiver. This includes the short cables on the PP and synchronizer chassis.

SIGNAL TIMING



Notes:

(A) Total Turnaround Time between Function and Inactive measured at the PPS should be 410 ns ± 35 ns to maintain 500 ns Cycle Time.

(B) All inputs from the Channel to the PPS must arrive at the PP in the 75 ns window indicated, to avoid lost data (inputs may be earlier or later by 100 ns multiples).

(C) All AC Transmission Pulse Widths are 25 ns ± 5 ns.

Similar timing relationships exist for Data, Full, Empty, etc.

The MASTER CLEAR is pulsed at 4096-μsec periods for as long as the DEADSTART switch (on the deadstart panel) is in the ON position, or while the DEADSTART button (on the display console) is pressed. Each deadstart cycle causes a train of pulses to be transmitted, on all channels, for a 1-μsec period.

SIGNAL RELAY

Signal relay is necessary in all synchronizers on a channel except in the one at the end of the line. Signal timing through the relay is at a 10 MHz rate. Each synchronizer appears as the processor to the next-in-line synchronizer except for a time lag. This time lag depends upon the cable length and the internal circuiting of each synchronizer between it and the data channel. Each synchronizer samples and stores all output signal lines in addition to sending them to the next-in-line synchronizer.

Each synchronizer also transfers all input signal lines to the next-in-line synchronizer. In addition, each synchronizer must provide for entering its signals onto the same lines. Therefore, the network feeding a processor (or the next-in-line synchronizer) is an 'OR' combination of the synchronizer and the one feeding it.

Computation of cable time and signal delay time through internal hardware allows a synchronizer to place the signals on the lines, for relay to the next-in-line synchronizer, at a time relative to the processor delayed by an integral multiple of 10MHz clock periods. Thus, each synchronizer appears as the processor to the next-in-line synchronizer.

TYPICAL DATA INPUT SEQUENCE

An external device sends data to the processor by way of a synchronizer in the following manner (refer to Figure 2-3).

1. The processor places a function word in the channel register and sets the 'full' and 'channel active' flags. Coincidentally it sends the function word and a 'function' signal to all synchronizers. The 'function' signal tells all synchronizers to sample the word and identifies it as a function code (as opposed to a data word). The code selects a synchronizer and a mode of operation. Nonselected synchronizers clear and only the selected synchronizer is turned on. A synchronizer eill not select if it detects a parity error in the function word.

2. The synchronizer sends an 'inactive' signal to the processor, indicating acceptance of the function code. This signal drops the 'channel active' flag which, in turn, drops the 'full' flag and clears the channel register.

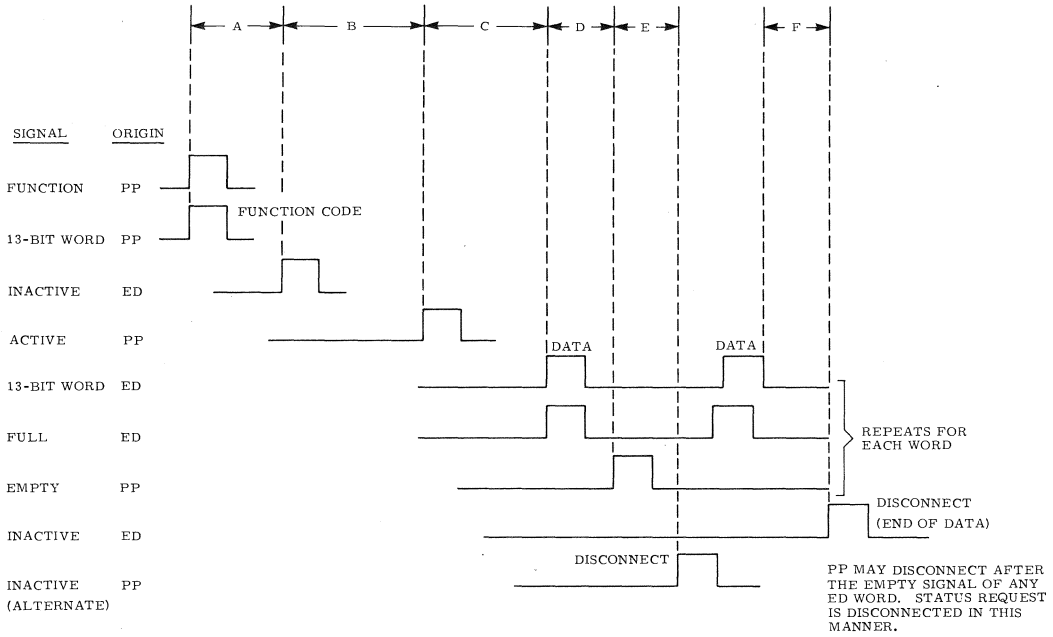
3. The processor sets the 'channel active' flag and sends an 'active' signal to the synchronizer signalling the device to start sending data.

4. The device reads a word and then sends that word to the channel register with a 'full' signal which sets the 'channel full' flag coincident with the data arrival.

5. The processor stores the word, drops the 'full' flag and returns an 'empty' signal indicating acceptance of the word. The device clears its data register and prepares to send the next word. The detection of a parity error by the channel causes a signal to be sent to the Status and Control Register, indicating this condition and the channel on which it occurred.

6. Steps 4 and 5 are repeated for each word transferred.

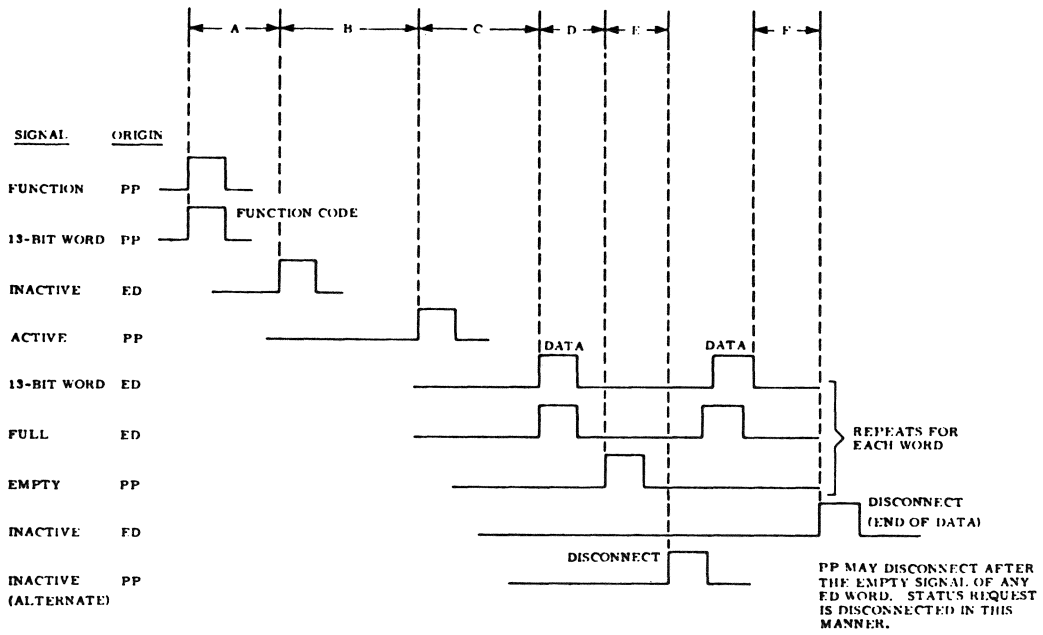
7. At the end of the transfer, the synchronizer clears its 'active' condition and sends an 'inactive' signal to the processor to indicate 'end-of-data'. The signal clears the 'channel active' flag, disconnecting the synchronizer and the processor from the channel.



PP = peripheral and control processor; ED = external device

A.	Time is a function of ED	PP recognizes inactive 1 microsecond after function or at an integral multiple thereafter.
B.	Time is a function of PP	Minimum time is 100 nanoseconds, actual time is a function of the PP program.
C.	Time is a function of ED	
D.	Time is a function of PP	Minimum time is 100 nanoseconds, maximum time is an integral multiple of 100 nanosecond intervals thereafter.
E.	Time is a function of PP	Minimum time is 3 major cycle times, maximum time is an integral multiple of 1 microsecond intervals thereafter.
F.	Time is a function of ED	

Figure 2-3(A). Data Input Sequence, Data Channel 1.0 μs Mode of Operation



PP = peripheral and control processor; ED = external device

A.	Time is a function of ED	PP recognizes inactive 0.5 microseconds after function or at an integral multiple thereafter. Inactive must have been received by the PP some time before this.
B.	Time is a function of PP	Minimum time is 50 nanoseconds, actual time is a function of the PP program.
C.	Time is a function of ED	
D.	Time is a function of PP	Minimum time is 50 nanoseconds, maximum time is an integral multiple of 50-nanosecond intervals thereafter (up to 450 nsec to allow 500-nsec mode of operation)
E.	Time is a function of PP	Minimum time is 1.5 microseconds, maximum time is an integral multiple of .5-microsecond intervals thereafter.
F.	Time is a function of ED	

Figure 2-3(B). Data Input Sequence, Data Channel 500 nsec Mode of Operation

8. As an alternative, the processor may choose to deactivate the channel before the device has sent all its data. The processor does this by dropping the 'active' flag and sending an 'inactive' signal to the synchronizer which immediately clears its active condition and sends no more data, although the device may continue to the end of its record or cycle (e.g., a magnetic tape unit continues to 'end-of-record' and stops in the record gap).

STATUS REQUEST

A status request is a special one-word data input transfer in which an external device indicates a 'ready' or 'error' condition to a processor (refer to Figure 2-3).

1. The processor places a function word in the channel register and sets the 'full' and 'channel active' flags. At the same time, it sends the word and a 'function' signal to all synchronizers. The 'function' signal tells all synchronizers to sample the word as a function code (as opposed to a data word). The code selects a synchronizer and places it in the 'status' mode. Nonselected synchronizers clear, and only the selected synchronizer is turned on. A synchronizer will not select if it detects a parity error.

2. The synchronizer sends an 'inactive' signal to the processor indicating acceptance of the status function code. The signal drops the 'channel active' flag which, in turn, drops the 'full' flag and clears the channel register.

3. The processor sets the 'channel active' flag and sends an 'active' signal to the synchronizer which signals the device to send the status word.

4. The synchronizer sends the status word, drops the 'full' flag and returns an 'empty' signal, indicating acceptance of the word. The detection of a parity error by the processor causes a signal to be sent to the Status and Control Register, indicating this condition and the channel on which it occurred.

5. The synchronizer accepts the word and sends an 'empty' signal to the processor where it clears the channel register and drops the 'full' flag.

6. The processor drops the 'channel active' flag and sends an 'inactive' signal to turn the synchronizer off.

TYPICAL DATA OUTPUT SEQUENCE

The processor sends data to an external device in the following manner (refer to Figure 2-4).

1. The processor places a function word in the channel register and sets the 'full' and 'channel active' flags. Coincidentally, it sends the word and a 'function' signal to all synchronizers. The 'function' signal informs all synchronizers to sample the word and identifies it as a function code. The code selects a synchronizer and a mode of operation. Nonselected synchronizers clear, and only the selected synchronizer is turned on. A synchronizer will not select if it detects a parity error in the function word.

2. The synchronizer sends an 'inactive' signal to the processor, indicating acceptance of the function code. The signal drops the 'channel active' flag which, in turn, drops the 'full' flag and clears the channel register.

3. The processor sets the 'channel active' flag and sends an 'active' signal to the synchronizer which signals to the device that data flow is starting.

4. The processor places a data word in the channel register and sets the 'full' flag. Coincidentally, it sends the word and a 'full' signal to the synchronizer.

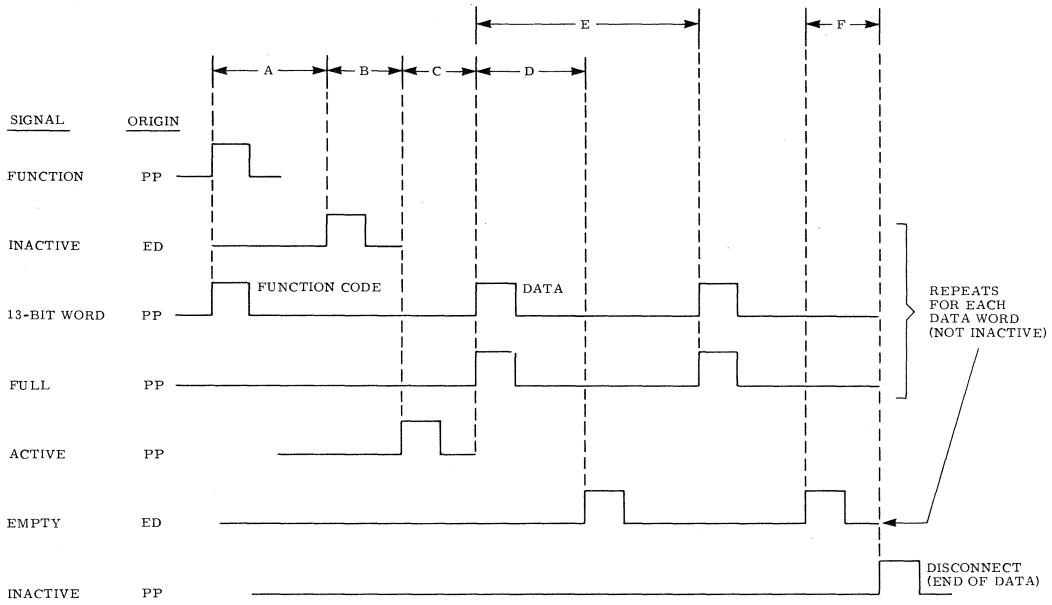
5. The synchronizer accepts the word and sends an 'empty' signal to the processor, where it clears the channel register and drops the 'full' flag.

6. Steps 4 and 5 are repeated for each synchronizer word.

7. After the last word has been transferred and acknowledged by the synchronizer, the processor drops the 'channel active' flag and sends an 'inactive' signal to the synchronizer, turning it off.

TREATMENT OF PARITY ERROR

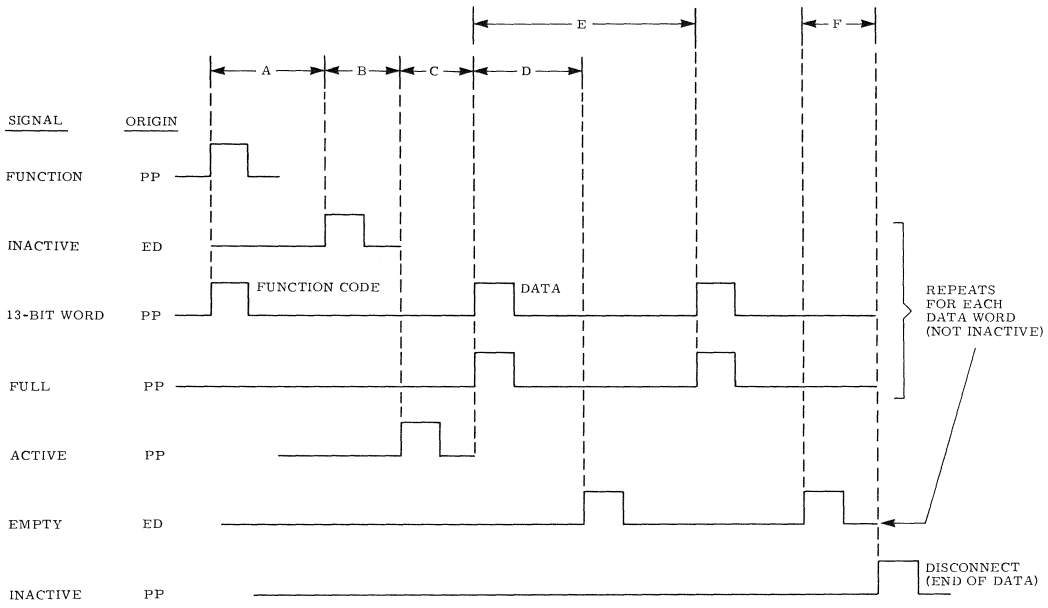
One odd parity bit is added to all the 12-bit words (data or function) prior to loading the channel output registers. Thus, a 13-bit word is transferred on the output channel. Likewise, a 13-bit word is expected on input transfers from the external devices. The incoming 13-bit words are held in the appropriate 'channel data-in' registers, where the odd parity is checked and only the 12 data bits are transferred to the appropriate register or registers. Parity bits are transferred over the 'W' wire in both input and output coaxial cables.



PP = peripheral and control processor; ED = external device

A.	Time is a function of ED	PP recognizes inactive 1 microsecond after function or at an integral multiple thereafter.
B.	Time is a function of PP	Minimum time is 100 nanoseconds, actual time is a function of the PP program.
C.	Time is a function of PP	Minimum time is 2 microseconds or 4 microseconds depending on instruction. Actual time is a function of the PP program.
D.	Time is a function of ED	
E.	Time is a function of ED	Minimum PP time is 1 microsecond.
F.	Time is a function of PP	Minimum time is 2 microseconds after empty from ED.

Figure 2-4(A). Data Output Sequence, Data Channel 1.0 µs Mode of Operation



PP = peripheral and control processor; ED = external device

A.	Time is a function of ED	PP recognizes inactive 0.5 microsecond after function or at an integral multiple thereafter.
B.	Time is a function of PP	Minimum time is 50 nanoseconds. Actual time is a function of the PP program.
C.	Time is a function of PP	Minimum time is 1 or 2 microseconds depending on instruction. Actual time is a function of the PP program.
D.	Time is a function of ED	(To allow 500-nsec mode of operation, minimum 50 nsec, maximum of 450 nsec.)
E.	Time is a function of ED	Minimum PP time is 0.5 microsecond.
F.	Time is a function of PP	Minimum time is 1 microsecond after empty from ED.

Figure 2-4(B). Data Output Sequence, Data Channel 500 nsec Mode of Operation

There is no parity on the control signals transferred to and from the peripheral processors on the channels.

In the event of a parity error during an input data transfer on any of the channels of a PPS, a parity error indication is sent to the Status and Control Register. Bits from 024 to 035 are set for the respective channel parity errors of the twelve channels. The PPS continues in its normal mode of operation, and any corrective action to retrieve the system is left to the system's software. If a transmission parity error occurs during an output transfer, it is expected that the external device synchronizers will set an error bit in their respective error registers. Any other action taken may vary from device to device depending upon its capabilities.

The internal Data Channel Converter (DCC), built as a component of AA107-A and AA120-A, on detecting a parity error on data transfer from the channel responds in the following manner:

1. Parity, Error in Function Codes
   (a) The 'connect' and 'function' signals to the 3000 series equipment are blocked.
   (b) The converter does not send an 'inactive' signal to the channel.
   (c) The parity error status bits 2^2 and 2^{11} in the converter are not set.
   (d) The Function is not executed.
2. Parity Error on Data Words (including functional data on Mode II Connect or Function)
   (a) Both parity error status bits 2^2 and 2^{11} are set in the converter status word.
   (b) The data is used as normal. The parity bit received from channel is sent unchanged to the 3000 series synchronizers. The connected synchronizer will also detect the parity error and react appropriately.

   To Mode II Connect or Function code parity errors, the DCC will generate an 'empty' signal after a delay of 100 nanoseconds.
3. Parity Error on Data Received by the DCC from the 3000 Series equipment
   (a) Bit 2^2 is set in the DCC status word.
   (b) The data is sent to the channel with uncorrected parity.

4. Parity on Status Information.

   No parity is generated on status information transferred from the 3000 Series equipment to the DCC. The DCC generates and transmits parity for the status information to the channel.

   For external devices with no parity capability, there are twelve switches on the PPS chassis to disable parity checking on data received on any of the twelve channels.

TEST OF PARITY SYSTEM

The capability to test the parity network in the PPS is provided via the Status and Control Register. A bit is provided (Bit 120_8) on the Status Control Register which forces zero parity transfer. This capability is not selectable for a single channel. Once the bit is set, it forces zero parity on all twelve channels.

CONTROLLER/EQUIPMENT CONNECTIONS 3

TYPICAL CONNECTIONS

Synchronizers are connected to an associated data channel as shown in the typical configuration in Figure 3-1.

Several synchronizers may be connected to a common data channel provided none have identical select function codes.

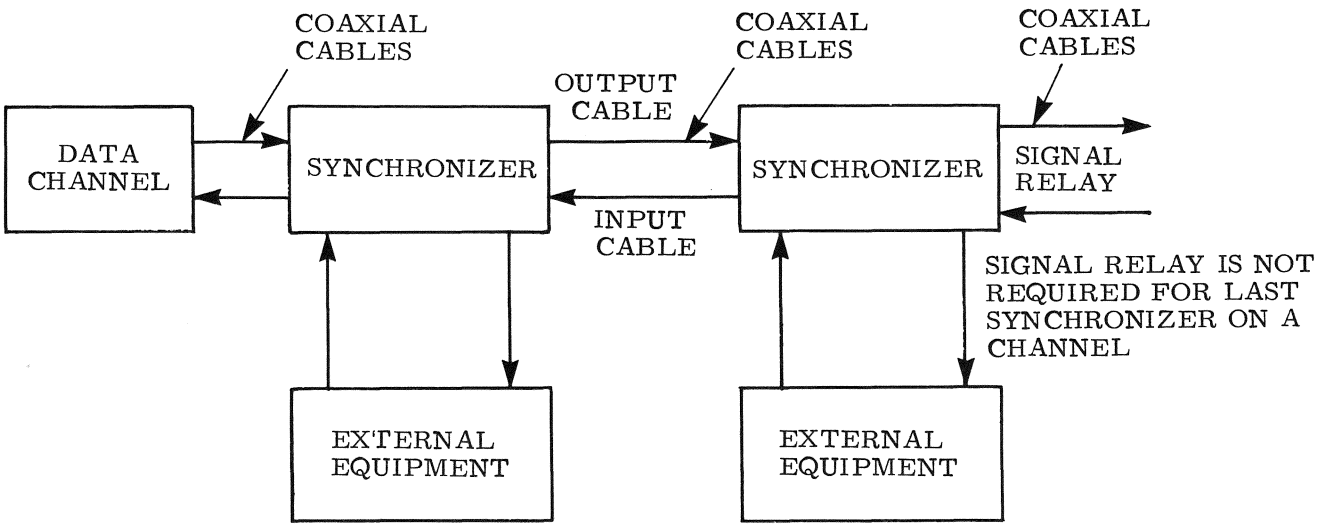


Figure 3-1. Typical Synchronizer/Equipment Connections

SPECIAL CONNECTIONS

Two special equipment have a modified configuration. These are the DCC data channel converter and the 6682/83 satellite coupler (refer to Figures 3-2 and 3-3).

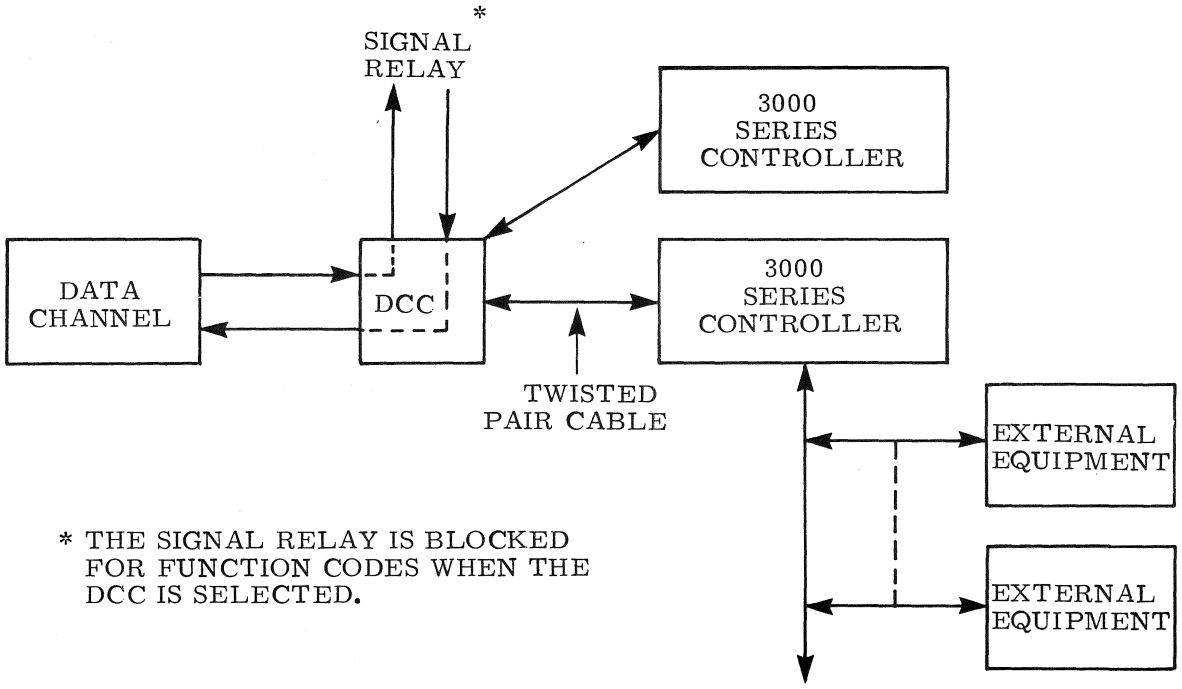


Figure 3-2. Typical DCC Configuration

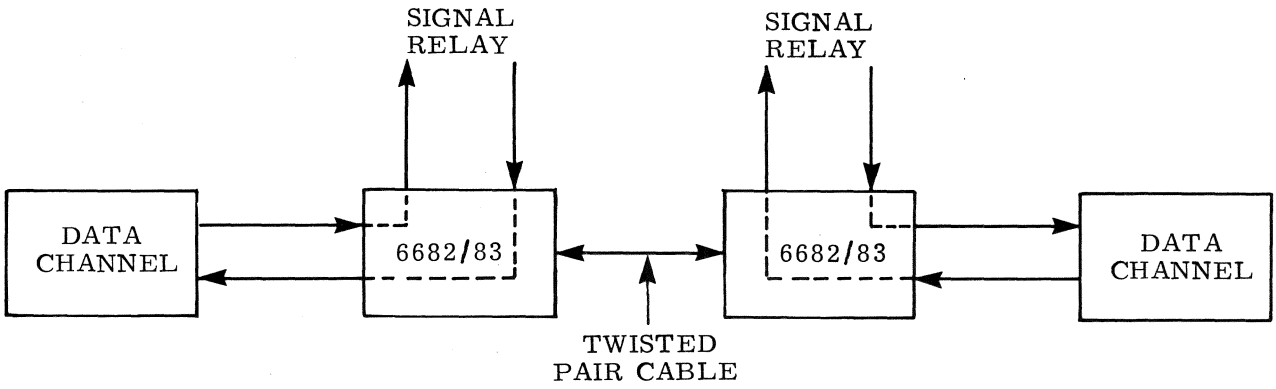


Figure 3-3. Typical 6682/83 Configuration

The 6681 may be selected by a select function code or by performing a master clear. The 6682/6683 and all other controllers may be selected by a select function code only.

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